What is claimed is:

1. A method of manufacturing semiconductor devices comprising the step of estimating, based on a replacement address for replacing with a redundancy circuit which address is stored in each of a plurality of semiconductor memory chips into which a wafer has been divided, position information of these semiconductor memory chips on said wafer.

2. A method of manufacturing semiconductor devices according to claim 1, wherein a distribution on said wafer of those semiconductor memory chips which have been determined as faulty by a semiconductor tester is determined based on said position information.

3. A method of manufacturing semiconductor devices according to claim 2, wherein a manufacturing device which causes a failure to a semiconductor memory chip in a manufacturing line is identified from said distribution.